Remarks

Reconsideration of the application is respectfully requested in view of the foregoing amendments and following remarks. Claims 1-37 are pending in the application. No claims have been allowed. New claim 37 has been added. Claims 1, 17, 30, 35, 36 and 37 are independent.

Response to Drawing Objections

Reference signs 95 and 370 have been deleted in Figures 2 and 5, respectively, and reference signs 480 and 545 have been removed from Figure 9. Applicant encloses herewith replacement sheets with these changes. Applicant respectfully requests approval of these changes.

Response to Specification Objections

The paragraph beginning at page 8, line 18 has been amended by changing "are BitByt selector 466" to --and BitByt selector 466--.

In the paragraph beginning at page 9, line 8, reference number 310 has been changed to 320, and reference number 320 has been changed to 310.

Applicant respectfully requests approval of these changes.

Response to § 112, First Paragraph Rejection

In the Action, the Examiner objects to claim 35 under 35 U.S.C. § 112, first paragraph. The Examiner states, "Specifically, the claim recites selecting an analog circuit which the claim types as being a filter. The examiner does not know what kind of filter the applicant has in mind that would qualify to be an analog circuit, and the specification does not teach this circuit. Applicant respectfully traverses this rejection.

As stated in the M.P.E.P., "There is a strong presumption that an adequate written description of the claimed invention is present when the application is filed." [*See* M.P.E.P. § 2163, p. 2100-166.] Further, "The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement." [*See* M.P.E.P. § 2163.02.] For example, "What is conventional or well known to

one of ordinary skill in the art need not be disclosed in detail." [*See* MPEP § 2163 at p. 2100-172.]

The word "filter" appears in original claim 35. Although the word "filter" does not appear in the specification other than in the claims, analog filters in mixed-signal circuits are well-known in the art. For example, in Chatterjee and Nagi, "Design for Testability and Built-In Self-Test of Mixed-Signal Circuits: A Tutorial," *IEEE 10th Int'l Conference on VLSI Design*, pp. 388-92 (January 1997) (previously cited by Applicant in an Information Disclosure Statement dated April 23, 2002), the authors discuss, e.g., active filters with cascaded stages and switched-capacitor filters. [*See id.* at p. 388.] The term "filter" in claim 35 is not limited to the filters described in Chatterjee and Nagi, but such a description shows that different kinds of analog filters in mixed-signal circuits are well-known in the art. Therefore, filters "need not be disclosed in detail." [*See* MPEP § 2163 at p. 2100-172.]

The § 112, first paragraph rejection of claim 35 should be withdrawn. Such action is respectfully requested.

Response to § 112, Second Paragraph Rejections

Claim 7 has been amended to read, "The integrated circuit of claim 1 wherein the memory is of a type selected from the group including at least: read-only memory, programmable read-only memory, random access memory."

Claim 10 has been amended to depend from claim 9, which recites a test controller module.

Claim 34 has been amended to read, "The integrated circuit of claim 30 further comprising: means for selecting a condition checker."

Claim 35 has been amended to read in part, "wherein the selected analog node is of a type selected from a group including at least: an analog-to-digital converter, a digital-to-analog converter, and a filter."

Claim 36 has been amended to read in part, "transmitting instructions for testing circuitry wherein the instructions include instructions for . . . ."

The § 112, second paragraph rejections of claims 7, 10, 34, 35 and 36 should be withdrawn. Such action is respectfully requested.

Applied Art

U.S. Patent No. 6,536,006 to Sugamori ("Sugamori") is entitled "EVENT TESTER ARCHITECTURE FOR MIXED SIGNAL TESTING." U.S. Patent No. 5,557,052 to Morris ("Morris") is entitled "SCAN BASED TESTING FOR ANALOGUE CIRCUITRY." U.S. Patent No. 5,659,312 to Sunter et al. ("Sunter") is entitled "METHOD AND APPARATUS FOR TESTING DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS." U.S. Patent No. 6,532,561 to Turnquist et al. ("Turnquist") is entitled, "EVENT BASED SEMICONDUCTOR TEST SYSTEM."

Rejection of Claims 17-19, 27-29 and 36 over Sugamori Under § 102(e)

The Action rejects claims 17-19, 27-29 and 36 under 35 U.S.C. § 102(e) as being anticipated by Sugamori. Applicant respectfully traverses these rejections. For a 102(e) rejection to be proper, the applied art must teach each and every element as set forth in a claim. (*See* MPEP § 2131.01.) However, the applied art does not teach each and every element of claims 17-19, 27-29 and 36.

Claims 17-19 and 27-29

Sugamori does not teach or suggest, for example, "A method for testing an integrated circuit having multiple analog nodes and testing circuitry, comprising . . . comparing the test value of the selected analog node with the tolerance value, wherein the comparing is performed by a condition checker in the testing circuitry, the condition checker performing comparisons of test values and tolerance values for plural analog nodes in the integrated circuit," as recited in amended independent claim 17.

As amended, independent claim 17 recites:

> A method for testing *an integrated circuit having multiple analog nodes and testing circuitry*, comprising:
> selecting an analog node in the integrated circuit from a list of analog nodes stored in a memory;
> obtaining a test value from the selected analog node;
> retrieving a tolerance value associated with the selected analog node from a memory; and
> comparing the test value of the selected analog node with the tolerance value, wherein the comparing is performed by a condition checker in the testing

circuitry, the condition checker performing comparisons of test values and tolerance values for plural analog nodes in the integrated circuit.

In the Action, the Examiner rejects claim 17 under § 102(e). Applicant respectfully disagrees.

First, Sugamori does not teach an integrated circuit having multiple analog nodes and testing circuitry, as recited in amended claim 17. Instead, Sugamori is understood to describe event tester boards and an *entirely separate* device under test that can be tested by the event tester boards. [*See* Sugamori at Fig. 4.] Although Sugamori describes "testing the analog functions of the device under test" [*see* Sugamori at column 8, lines 1-2], Sugamori does not teach "an integrated circuit having multiple analog nodes *and testing circuitry*," as recited in amended claim 17. The tester boards of Sugamori are not even partially contained in Sugamori's device under test. Therefore, the claim 17 requirement of "an integrated circuit having multiple analog nodes and testing circuitry" is not found in Sugamori.

Second, claim 17 recites "retrieving a tolerance value associated with the selected analog node from a memory; and comparing the test value of the selected analog node with the tolerance value, wherein the comparing is performed at least in part by the testing circuitry." The Examiner cites col. 8, lines 13-18 and lines 61-67 as purportedly showing the retrieving of a tolerance value associated with a selected analog node from a memory. [*See* the Action at page 5.] The passages cited by the Examiner are understood to describe an "event execution unit" that produces a "test pattern based on the event data from the event memory," [*see* Sugamori at col. 8, lines 13-18] but the described "test pattern" is not understood to relate to "tolerance values." Sugamori is not understood to describe "tolerance values" in the cited passages or anywhere else, and therefore does not teach "comparing the test value of the selected analog node with the tolerance value," as recited in claim 17. In addition, Sugamori does not teach that such "comparing is performed by a condition checker in the testing circuitry, the condition checker performing comparisons of test values and tolerance values for plural analog nodes in the integrated circuit," as also recited in claim 17.

Because Sugamori does not teach or each an every element of independent claim 17, the rejection of claim 17 under 35 U.S.C. § 102(e) should be withdrawn. Such action is respectfully requested.

Claims 18-19 and 27-29 depend from claim 17 and are allowable for the reasons given above in support of their parent claim 17. These claims are also each independently patentable. For example, claim 28 recites in part, "prior to the comparing, selecting a condition checker in the testing circuitry for performing the comparing." Accordingly, the rejection of claims 18-19 and 27-29 under 35 U.S.C. § 102(e) also should be withdrawn. Such action is respectfully requested.

Claim 36

Sugamori does not teach or suggest, for example, "comparing the test value of the selected analog node with the tolerance value, wherein the comparing is performed at least in part by testing circuitry within the integrated circuit," as recited in independent claim 36, as amended.

As amended, independent claim 36 recites:

> A computer-implemented method, comprising:
> transmitting instructions for testing circuitry wherein the instructions include instructions for:
> selecting an analog node in an integrated circuit from a list of analog nodes stored in a memory of the integrated circuit;
> obtaining a test value from the selected analog node;
> retrieving a tolerance value associated with the selected analog node from a memory; and
> comparing the test value of the selected analog node with the tolerance value; wherein the comparing is performed at least in part by testing circuitry within the integrated circuit.

Sugamori is not understood to teach anything relating to tolerance values and thus does not teach or suggest "retrieving a tolerance value associated with the selected analog node from a memory" or "comparing the test value of the selected analog node with the tolerance value; wherein the comparing is performed at least in part by testing circuitry within the integrated circuit," as recited in amended claim 36.

Because Sugamori does not teach at least one element of independent claim 36, the rejection of claim 36 under 35 U.S.C. § 102(e) should be withdrawn. Such action is respectfully requested.

Rejection of Claims 1-16, 20-26 and 30-35 Under § 103

The Action rejects claims 1-7, 9-11, 13-16, 30 and 33-35 under 35 U.S.C. § 103(a) in view of Sugamori, claim 8 in view of Sugamori and Morris, claim 12 in view of Sugamori and Sunter, and claims 20-26 and 31-32 in view of Sugamori and Turnquist. Applicant respectfully traverses these rejections.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2142.) Applicant respectfully submits that the claims in their present form are allowable over the applied art because they do not teach or suggest all the claim limitations of claims 1-16, 20-26 and 30-35.

Claims 1-7, 9-11, 13-16, 30 and 33-35

In the Action, the Examiner rejects claims 1-7, 9-11, 13-16, 30 and 33-35 under § 103(a) in view of Sugamori. Applicant respectfully disagrees.

Sugamori does not teach or suggest, for example, "An integrated circuit comprising testing circuitry and core logic circuitry, comprising: a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes" and "a condition checker that compares actual test values of the analog nodes with the associated tolerance values," as recited in independent claim 1.

Independent claim 1 recites:

> An integrated circuit comprising testing circuitry and core logic circuitry, comprising:
> a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes;
> a condition checker that compares actual test values of the analog nodes with the associated tolerance values; and
> a main control unit coupled to the memory and the condition checker that synchronizes testing of the core logic circuitry.

The Examiner states at page 8 of the Action, "Sugamori however does not teach the above features as all being part of an integrated circuit, rather the system is composed of a tester board plus filter and the CUT and consists of two separate units." The Examiner asserts that claim 1 is nevertheless obvious, stating:

> But it would have been obvious to one with ordinary skill in the art at the time of the invention, to combine the system into one integrated circuit, because it would have been an obvious design choice. And one would have been motivated by cost

> and speed of test to integrate the system of Sugamori, in the same manner that all improvements and miniaturizations occur every day in the art of integrated circuits.

[*See* the Action at page 8.] Applicant respectfully disagrees, for several reasons.

First, even taken together, the "separate units" of Sugamori do not teach or suggest each and every element of the integrated circuit of claim 1. For example, claim 1 recites "a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes." The Examiner takes the position that the memory 68 and event memory 60 of Sugamori describe this cited language of claim 1. However, Sugamori does not describe "tolerance values," let alone teaching or suggesting "a memory that stores . . . tolerance values associated with the analog nodes."

The integrated circuit of claim 1 comprises "a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes; a condition checker that compares actual test values of the analog nodes with the associated tolerance values; and a main control unit coupled to the memory and the condition checker that synchronizes testing of the core logic circuitry." These requirements are not understood to be shown or suggested by Sugamori. In contrast, Sugamori describes event tester boards and a separate device under test that can be tested by the event tester boards. [*See* Sugamori at Fig. 4.] The integrated circuit of claim 1 is not merely a "one-piece construction" of the separate units described in Sugamori that have been "rigidly secured together as a single unit," as was the situation in the *In re Larson* case cited by the Examiner. Claim 1 is simply not obvious in view of Sugamori.

Furthermore, Sugamori teaches away from the integrated circuit of claim 1. Sugamori states,

> Since the semiconductor test system of the present invention has a modular structure, a desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test.

[*See* Sugamori at col. 12, lines 23-26.] Thus, Sugamori favors separate, modular tester boards, which can be "formed freely depending on the kind of devices to be tested," and teaches away from the integrated circuit comprising testing circuitry as set forth in claim 1.

Because Sugamori does not teach or suggest at least one element of independent claim 1, the rejection of claim 1 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Claims 2-7, 9-11 and 13-16 depend from claim 1 and should be allowable for the reasons given above in support of claim 1. These claims are also independently patentable. For example, claim 5 recites in part, "the testing circuitry further comprises a second memory for storing diagnostic data." As another example, claim 16 recites in part, "means for selecting a condition checker from the plurality of condition checkers in the testing circuitry to compare a test value with an associated tolerance value." Accordingly, the rejection of claims 2-7, 9-11 and 13-16 under 35 U.S.C. § 103(a) also should be withdrawn. Such action is respectfully requested.

Claims 30 and 33-34

The Examiner has also rejected claims 30 and 33-34 under § 103(a) in view of Sugamori. Applicant respectfully disagrees.

Independent claim 30 recites:

> An integrated circuit comprising testing circuitry and core logic circuitry, wherein the testing circuitry comprises:
> means for selecting an analog node in the core logic circuitry from a list of analog nodes stored in a memory;
> means for obtaining a test value from the selected analog node;
> means for retrieving a tolerance value associated with the selected analog node from a memory; and
> means for checking whether the test value of the selected analog node is within the associated tolerance value.

In addition to other differences, Sugamori is not understood to describe tolerance values and therefore does not teach or suggest "means for retrieving a tolerance value associated with the selected analog node from a memory; and means for checking whether the test value of the selected analog node is within the associated tolerance value," as recited in independent claim 30.

Therefore, the rejection of claim 30 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Claims 33-34 depend from claim 30 and should be allowable for the reasons given above in support of their parent claim. These claims are also independently patentable. For example, claim 34 recites in part, "means for selecting a condition checker." Accordingly, the rejection of

claims 33-34 under 35 U.S.C. § 103(a) also should be withdrawn. Such action is respectfully requested.

Claim 35

The Examiner rejects claim 35 under § 103(a) in view of Sugamori. Applicant respectfully disagrees.

Independent claim 35 recites:

> A method for testing an integrated circuit having multiple analog nodes and testing circuitry, the method comprising:
> selecting an analog node in the integrated circuit from a list of analog nodes stored in a memory in the testing circuitry;
> obtaining a test value from the selected analog node;
> retrieving a tolerance value associated with the selected analog node from a memory in the testing circuitry; and
> comparing the test value of the selected analog node with the tolerance value;
> wherein the selected analog node is of a type selected from a group including at least: an analog-to-digital converter, a digital-to-analog converter, and a filter.

In addition to other reasons, Sugamori is not understood to describe tolerance values, and therefore does not teach or suggest "retrieving a tolerance value associated with the selected analog node from a memory in the testing circuitry; and comparing the test value of the selected analog node with the tolerance value," as recited in independent claim 35. Therefore, the rejection of claim 35 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Claim 8

In the Action, the Examiner rejects dependent claim 8 under § 103(a) on the basis of Sugamori in view of Morris. Applicant respectfully disagrees.

Even in combination, Sugamori and Morris do not teach or suggest each and every element of the integrated circuit of claim 8. For example, claim 8 recites in part, "the testing circuitry is JTAG-compliant." Although Morris describes a test access port and a test bus (e.g., at col. 9, line 54 - col. 10, line 5, as cited by the Examiner), Morris does not mention JTAG or JTAG compliance.

In addition, claim 1, from which claim 8 depends, recites "a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes." Sugamori does not describe "tolerance values," and Morris also does not describe "tolerance values." Therefore, Sugamori and Morris, either alone or in combination, do not teach a memory that stores tolerance values associated with analog nodes in an integrated circuit.

Because Sugamori and Morris do not teach or suggest at least one element of dependent claim 8, the rejection of claim 8 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Claim 12

In the Action, the Examiner rejects dependent claim 12 under § 103(a) on the basis of Sugamori in view of Sunter. Applicant respectfully disagrees.

Even in combination, Sugamori and Sunter do not teach or suggest each and every element of the integrated circuit of claim 12. For example, claim 1, from which claim 12 depends, recites "a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes." Neither Sugamori nor Sunter describe "a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes." Therefore, Sugamori and Sunter, either alone or in combination, do not teach a memory that stores tolerance values associated with analog nodes in an integrated circuit.

In addition, claim 12 recites in part, "the condition checker further comprises noise calibration circuitry." Although Sunter describes "low-pass filtering" and "noise reduction" (e.g., at col. 1, lines 41-43, as cited by the Examiner) and noise measurements (e.g., at col. 2, lines 55-56), neither Sunter nor Sugamori describes a condition checker that comprises noise calibration circuitry.

Because Sugamori and Sunter do not teach or suggest at least one element of dependent claim 12, the rejection of claim 12 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Claims 20-26 and 31-32

In the Action, the Examiner rejects claims 20-26 and 31-32 under § 103(a) on the basis of Sugamori in view of Turnquist. Applicant respectfully disagrees.

Sugamori in view of Turnquist does not teach or suggest each and every element of dependent claims 20-26. For example, claim 17, from which claims 20-26 depend, recites in part, "A method for testing an integrated circuit having multiple analog nodes and testing circuitry, comprising . . . comparing the test value of the selected analog node with the tolerance value, wherein the comparing is performed by a condition checker in the testing circuitry, the condition checker performing comparisons of test values and tolerance values for plural analog nodes in the integrated circuit." Sugamori in view of Turnquist does not have or suggest the recited language of independent claim 17.

Because Sugamori and Turnquist do not teach or suggest at least one element of independent claim 17, claims 20-26 are allowable in view of the allowability of their parent claim. These claims are also independently patentable. For example, claim 21 recites in part, "reconfiguring a memory in the integrated circuit to be operable to store diagnostic data from the testing circuitry." As another example, amended claim 23 recites in part, "storing data identifying the selected analog node in a data memory in the testing circuitry; and storing the test value of the selected analog node in a data memory in the testing circuitry. Therefore, the rejection of claims 20-26 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

With regard to claims 31 and 32, Sugamori in view of Turnquist does not teach or suggest each and every element of dependent claims 31-32. For example, claim 30, from which claims 31-32 depend, recites in part, "means for retrieving a tolerance value associated with the selected analog node from a memory; and means for checking whether the test value of the selected analog node is within the associated tolerance value." Sugamori in view of Turnquist does not have or suggest the recited language of independent claim 30.

Because Sugamori and Turnquist do not teach or suggest at least one element of independent claim 30, claims 31-32 are allowable in view of the allowability of their parent claim 30. These claims are also independently patentable. Therefore, the rejection of claims 31-32 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Request For Interview

If any issues remain, the Examiner is formally requested to contact the undersigned attorney prior to issuance of the next Office Action in order to arrange a telephonic interview. It is believed that a brief discussion of the merits of the present application may expedite prosecution. Applicant submits the foregoing formal Amendment so that the Examiner may fully evaluate Applicant's position, thereby enabling the interview to be more focused.

This request is being submitted under MPEP § 713.01, which indicates that an interview may be arranged in advance by a written request.

Conclusion

The claims in their present form should now be allowable. Such action is respectfully requested.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By _____
David P. Petersen
Registration No. 28,106

One World Trade Center, Suite 1600
121 S.W. Salmon Street
Portland, Oregon 97204
Telephone: (503) 226-7391
Facsimile: (503) 228-9446

Amendments to the Drawings

The attached sheets of drawings include changes to Figures 2, 5 and 9, as described in the following remarks. These sheets replace the original sheets of drawings.

Attachment: Replacement sheets